

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A method of performing a dot
2 product operation with rounding and shifting in a microprocessor in
3 response to a single rounding dot product instruction, the method
4 comprising the steps of:

5 fetching a first pair of elements and a second pair of
6 elements;

7 forming a first product of the first pair of elements and a
8 second product of the second pair of elements;

9 combining the first product with the second product to form a
10 combined product and rounding the combined product to form an
11 intermediate result via an arithmetic circuit having a first input
12 receiving said first product, a second input receiving said second
13 product and a carry input to a mid-position receiving said rounding
14 value to form the intermediate result; and

15 right shifting the intermediate result a selected amount to
16 form a final result.

Claims 2 and 3. (Canceled)

1 4. (Previously Presented) The method of Claim 1, wherein the
2 rounding value is 2^n and the selected shift amount is $n+1$.

1 5. (Original) The method of Claim 4, wherein n has a fixed
2 value of fifteen.

Claims 6 to 8. (Canceled)

1 9. (Previously Presented) The method of Claim 1, wherein the
2 steps of forming the first product and forming the second product
3 treats a one of the first pair of elements as a signed number value
4 and treats another one of the first pair of elements as an unsigned
5 number value.

1 10. (Original) The method of Claim 1, wherein the step of
2 combining comprises subtracting the product of second pair of
3 elements from the product of first pair of elements.

1 11. (Original) The method of Claim 1, wherein the step of
2 combining comprises adding the product of second pair of elements
3 to the product of first pair of elements.

12. (Canceled)

1 13. (Previously Presented) A digital system having a
2 microprocessor operable to execute a rounding dot product
3 instruction, wherein the microprocessor comprises:
4 storage circuitry for holding pairs of elements;
5 a multiply circuit connected to receive a first number of
6 pairs of elements from the storage circuitry in a first execution
7 phase of the microprocessor responsive to the dot product
8 instruction, the multiply circuit comprising a plurality of
9 multipliers equal to the first number of pairs of elements;
10 an arithmetic circuit having a plurality of inputs each
11 connected to receive a corresponding one of the plurality of
12 products from the plurality of multipliers and a mid-position carry
13 input for mid-position rounding responsive to the rounding dot
14 product instruction; and

15 a shifter connected to receive an output of the arithmetic
16 circuit, the shifter operable to shift a selected amount in
17 response to the rounding dot product instructions.

Claims 14 and 15. (Canceled)

1 16. (Currently Amended) The method of Claim 1, wherein:
2 the step of shifting further includes sign extending the
3 intermediate result.

1 17. (New) The digital system of Claim 13, wherein:
2 the shifter right shifts the output of the arithmetic circuit
3 by the selected amount and sign extends the output of the
4 arithmetic circuit.

18 to 24. (Canceled)